REMARKS

Claims 1-16 were pending in the application. The Examiner has rejected Claims 1-8 under 35 USC 102(b) as anticipated by Chiu; has objected to Claims 9-16 under 37 CFR 1.75(c) as being in improper form; and has not addressed the language of Claims 9-16 on the merits.

Applicants respectfully assert that revised claims, numbered 1-13, had been submitted in the original U.S. filing on August 15, 2006. However, since the revised claims were not entered into the record, Applicants herein amend Claim 1, cancel Claims 2, and 7- -16, and introduce new Claims 17-28. No new matter in introduced by the amendments. Applicants believe that no additional filing fees are due for introduction of the new claims, since the total number of claims does not exceed 20 and there are only two independent claims. Should any fee be required for this submission, authorization is hereby given to charge Deposit Account 50-0510.

For the reasons set forth below, Applicants believe that the claims, as amended, are patentable over the cited art. The present invention provides a method for fabricating a multilevel structure or an integrated circuit

having a multilevel interconnection structure, the method comprising steps of depositing a curable liquid layer on a substrate surface, aligning the stamp relative to the substrate surface; pressing a stamp having a multilevel pattern therein into the liquid layer to produce in the liquid layer a multilevel structure defined by the pattern; curing the liquid layer to produce a multilevel patterned mask in said solid layer having the multilevel structure therein; removing the stamp; and performing at least one subtractive processing through said multilevel patterned mask to pattern said substrate. For the integrated circuit having a multilevel interconnection structure, the method further comprises forming an electrically conductive structure between at least one pair of adjacent levels of the interconnection structure by performing at least one additive processing to deposit conductive material thereon.

The Chiu patent is directed to forming a series of ceramic ridges in alignment with patterned features on a substrate. Under the Chiu patent teachings, a ceramic slurry with binder is applied to a patterned mold, the mold is applied to the substrate, with the features of the patterned mold being aligned to the patterned features on the substrate. While the mold is still in place, the binder is cured. The mold is then removed, leaving a

patterned green state ceramic in place adhered to the substrate. Thereafter, the green state ceramic is sintered to form the final patterned ceramic structure.

Applicants assert note that Chiu is directed to forming a permanent patterned layer, while the present invention is directed to providing a removable patterned mask for forming multilevel interconnect structures. As set forth in the present Specification, the prior art methods for forming multilevel interconnect structures, such as dual damascene processing, require multiple costly steps and waste of multiple layers of sacrificial mask materials. The present invention provides a method for forming the multilevel interconnect structures by forming the multilevel mask in situ and then processing the substrate through the multilevel mask. The Chiu patent neither teaches nor suggests processing, additive or subtractive processing, of the underlying substrate through the formed multilevel mask to obtain a multilevel interconnect structure. Applicants have amended the language of the independent claim, Claim 1, to expressly recite the processing through the multilevel patterned mask structure, as supported in the original Specification (see: e.g., page 7, line 33-page 8, line 21 and page 9, lines 16-24).

Applicants respectfully contend that the Chiu patent neither teaches nor suggests the invention as claimed. With reference to the claim language, Chiu does not teach a method for fabricating a multilevel patterned mask structure on a surface (Claims 1) or a method for fabricating an integrated circuit having a multilevel interconnection structure (Claim 28). While Chiu does teach depositing a curable liquid layer on a substrate surface; pressing a stamp having a pattern into the liquid layer to produce in the liquid layer a structure defined by the pattern; and curing the liquid layer to produce a patter in the solid layer, Chiu does not teach or suggest those steps for forming a multilevel patterned mask, along with the steps of removing the stamp and performing at least one subtractive processing through said multilevel patterned mask to pattern the substrate (Claim 1 and claims which depend therefrom) or performing at least one additive processing to deposit conductive material on the substrate (Claim 28).

Anticipation under 35 USC 102 is established only when a single prior art reference discloses each and every element of a claimed invention. See: In re Schreiber, 128 F. 3d 1473, 1477, 44 USPQ2d 1429, 1431 (Fed. Cir. 1997); In re Paulsen, 30 F. 3d 1475, 1478-1479, 31 USPQ2d 1671, 1673

(Fed. Cir. 1994); In re Spada, 911 F. 2d 705, 708, 15 USPQ2d 1655, 1657 (Fed. Cir. 1990) and RCA Corp. v. Applied Digital Data Sys., Inc., 730 F. 2d 1440, 1444, 221 USPQ 385, 388 (Fed. Cir. 1984). Since the Chiu reference does not teach all of the claimed features, it cannot be concluded that Chiu anticipates the invention as claimed.

Based on the foregoing amendments and remarks, Applicants respectfully request entry of the amendment, reconsideration of the rejections, and issuance of the claims.

Respectfully submitted,

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